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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,195	12/21/2000	Toshiyuki Hirota	040373/0300	7014

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,195	HIROTA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-16,18-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-16,18-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 11-16, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of US Patent No. 6,326,270 to Lee et al. and US Patent No. 6,333,233 to Kojima.

AAPA (figures 1-7) teaches a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region (cell array region) containing transistor elements arrayed at a high density and a low-density region (peripheral circuit region) containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film (115) on a surface of the semiconductor substrate (101);

forming gate electrodes (116) on a surface of the gate oxide film (115), and forming oxide film (119) on the gate electrodes (116);

uniformly forming a first nitride film (131) having a predetermined thickness on the surface with the gate electrodes (116) formed thereon;

masking the high density region of the semiconductor substrate (101), and etching the first nitride film (131) in only the low density region to expose the gate oxide film (115) in gaps between the gate electrodes (116);

forming contact electrodes (122) connected to the semiconductor substrate (101) in the contact holes (121).

AAPA differs from the claimed invention by not showing annealing the semiconductor device formed so far in an atmosphere containing water vapor and annealing the semiconductor device formed so far with a forming gas to recover an interfacial level. Annealing the semiconductor device is well known in the art as shown for example by US Patent No. 5,930,584 to Sun et al. (column 3, lines 13-21). It would have been obvious to one having ordinary skill in the art at the time the invention was made for annealing the semiconductor device formed so far in an atmosphere containing water vapor because it eliminates the contamination, recover the defect, repair substrate damage, activate dopants, form silicide and other reasons. Additionally, it is also well known in the art to perform annealing steps at different times during fabrication.

AAPA differs from the claimed invention by not showing uniformly forming a second nitride film having a predetermined thickness on the low density region, the second nitride film also being uniformly formed on the first nitride film on the high density region. However, Lee et al. (figure 3A-G, 5) teach uniformly forming a second nitride film (119) having a predetermined thickness on the low density region (peripheral region), the second nitride film (119) also being uniformly formed on the first nitride film (112) on the high density region (cell array region). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee et al. into the device taught by Admitted Prior Art because it protects the gate electrode against over etching.

The combined device shows that forming an interlayer insulating film (133) on the second nitride (Lee et al.; 119) with an impurity introduced therein on a surface of the second nitride film.

The combined device shows that self-aligning the high-density region using the first nitride film (131) positioned on sides of the gate electrodes (116) as an etching stopper to form contact holes (122) reaching the semiconductor substrate (101) in the interlayer insulating film (133), wherein portions of the second nitride film (Lee et al.; 119) that are in direct contact with the first nitride film (112) and that are positioned on at least one of the respective sides of the gate electrodes (116) are removed as a result of the self aligning step.

AAPA and Lee et al. differ from the claimed invention by not showing forming an oxide film on the planarized top surface of the interlayer insulating film; and in the high density region, masking the oxide film, wherein the step of planarizing a top surface of the interlayer insulating film is performed before the step of self-aligning the high density region. However, Kojima (figures 3A-I) teaches forming an oxide film (26) on the planarized top surface of the interlayer insulating film (25); and in the high density region, masking the oxide film (27), wherein the step of planarizing a top surface of the interlayer insulating film (25) is performed before the step of self-aligning the high density region. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kojima into the device taught by AAPA and Lee et al. because it protects the surface of the device from the external environment. The combined device shows forming an oxide film on the planarized top surface of the interlayer insulating film; and in the high density region, masking the oxide

film, wherein the step of planarizing a top surface of the interlayer insulating film is performed before the step of self-aligning the high density region.

AAPA, Lee et al. and Kojima differ from the claimed invention by not showing the step of planarizing a top surface of the interlayer insulating film is performed after the step of annealing. The step of planarizing a top surface of the interlayer insulating film is performed after the step of annealing is a known in the art as shown for example by US Patent No. 6,198,143 to Ohsaki (column 7, lines 37-42). It would have been obvious to one having ordinary skill in the art at the time the invention was made for the step of planarizing a top surface of the interlayer insulating film is performed after the step of annealing because it eliminates the contamination, recovers the defect, repairs the damage, active dopants and other reasons. Additionally, it is also well known in the art to perform annealing steps at different time during fabrication.

Regarding claims 2 and 12, AAPA, Lee et al. and Kojima differ from the claimed invention by not showing the first nitride film and the second nitride film is formed by a CVD. AAPA, Lee et al. and Kojima are silent with respect to how the nitride film is deposited. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming the nitride film by a CVD, since it is a well known method of forming in the art.

Regarding claims 3 and 13, AAPA, Lee et al. and Kojima differ from the claimed invention by not showing the first nitride film is formed to a thickness ranging from 30 to 50 nm. Lee et al. teach a method, wherein the thickness of the first and second nitride films are formed to a thickness of about 20 –200 Angstroms (2-20 nm) (column 8, lines 1-3) and 50-150

Angstroms (5-15nm) (column 9, lines 37-38), respectively. Lee et al. teach a method, wherein the second nitride film is formed to a thickness ranging from 3.0 to 20 nm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm because it protects the surface of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 4 and 16, AAPA, Lee et al. and Kojima teach the first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning the high-density region.

It is inherent that the second nitride film is formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents the semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allow the forming gas to be diffused into the semiconductor substrate. They are known in the art as shown for example by JP02-87622, US Patent No. 5,116,768 to Kawamura (column 3, lines 25-31), and US Patent No. 4,927,770 to Swanson (abstract, lines 3-5).

Regarding claim 11, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 1.

AAPA further teaches etching the first nitride film (131) and gate oxide film (115) to expose the substrate (101) in gaps between gate electrodes (116) in the low-density region.

Regarding claim 14, AAPA, Lee et al. and Kojima differ from the claimed invention by not showing the first nitride film is formed by a chemical vapor deposition process, and the second nitride film is formed by a rapid thermal nitriding process. AAPA, Lee et al. and Kojima are silent with respect to how the first nitride film is deposited. It would have been obvious to select CVD, since it is a well-known method. Rapid thermal nitriding is a well known a method of forming nitride layer. It would have been obvious to select rapid thermal nitriding, since it is a well-known method.

Regarding claim 15, AAPA, Lee et al. and Kojima differ from the claimed invention by not showing the first nitride film is formed to a thickness ranging from 30 to 50 nm. Lee et al. teach a method, wherein the second nitride film is formed to a thickness of 2.0 nm (20 Angstroms; column 8, lines 1-3). It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm because it protects the surface of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 16, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 4.

Regarding claims 25 and 27, the combined device shows the second nitride film (Lee et al.; 119) only remains directly beneath the interlayer insulating film after the self-aligning step is completed.

3. Claims 6-9, 18-23, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Lee et al. in view of Kojima, and further in view of US Patent No. 5,807,779 to Liaw.

Regarding claim 6, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 1.

The combined device shows the nitride protective film (Lee et al.; 106), which is formed on the gate electrodes.

The combined device differs from the claimed invention by not showing to expose the nitride protective films on the gate electrodes. However, Liaw (figure 2) teaches to expose the nitride protective films (5) on the gate electrodes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Liaw into the device taught by AAPA, Lee et al. and Kojima because it uses to form contact hole on the gate electrode.

Regarding claim 7, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 2.

Regarding claim 8, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 3.

Regarding claim 9, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 4.

Regarding claim 18, the disclosures of AAPA, Lee et al., Kojima and Liaw are discussed as applied to claim 6.

AAPA further teaches etching the first nitride film (131) and gate oxide film (115) to expose the substrate (101) in gaps between gate electrodes (116) in the low-density region.

Regarding claim 19, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 7.

Regarding claim 20, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 8.

Regarding claim 21, AAPA, Lee et al., Kojima and Liaw differ from the claimed invention by not showing the first nitride film is formed by a chemical vapor deposition process, and the second nitride film is formed by a rapid thermal nitriding process. AAPA, Lee et al., Kojima and Liaw are silent with respect to how the first nitride film is deposited. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming the nitride film by a CVD, since it is a well known method of forming in the art. Rapid thermal nitriding is a well known a method of forming nitride layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select rapid thermal nitriding, since it is a well-known method.

Regarding claim 22, AAPA and Lee et al. differ from the claimed invention by not showing the first nitride film is formed to a thickness ranging from 30 to 50 nm, and the second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm. Lee et al. teach a method, wherein the thickness of the first and second nitride films are formed to a thickness of about 20 – 200 Angstroms (2-20 nm) (column 8, lines 1-3) and 50-150 Angstroms (5-15nm) (column 9, lines 37-38), respectively. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from

30 to 50 nm, and the second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm because it protects the surface of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 23, the disclosures of AAPA, Lee et al. and Kojima are discussed as applied to claim 9.

Regarding claims 26 and 28, the combined device shows the second nitride film (Lee et al.; 119) only remains directly beneath the interlayer insulating film after the self-aligning step is completed.

Response to Arguments

Applicant's arguments with respect to claims 1-4, 6-9, 11-16, 18-23 and 25-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
February 9, 2004

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